

- a processor circuit for executing program instructions;
- a memory interface for communicating with a main memory;

- a cache memory, the processing circuit servicing memory reading instructions from the cache memory in the cache mode, the processing circuit bypassing the cache for all memory reading instructions in the cache bypass mode;

- a power supply connection;

- 5 - a power supply switch coupled between the power supply connection and a power supply input of the cache memory, the power supply switch cutting off power supply to the cache memory in the cache bypass mode.

4. An apparatus that contains

- 10 - a data processing circuit switchable between operation in a cache mode and a cache bypass mode, the data processing circuit comprising a power supply connection, a cache memory and a power supply switch coupled between the power supply connection and a power supply input of the cache memory, the power supply switch cutting off power supply to the cache memory when the data processing circuit operates in the cache bypass mode

- 15 - a medium containing a program for the data processing circuit, the program containing a first and a second portion, and instructions for switching between the cache mode and the cache bypassing mode, so that the first portion is executed in the cache mode and the second portion is executed in the cache bypass mode, wherein execution of the first portion would not meet a real time constraint for operation of the apparatus if the first portion were executed
- 20 in the cache bypass mode.

5. A computer program product containing the program for the apparatus of Claim 4.

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